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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, THAN VINH	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,340	WARE ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,11,13,14,16-19,21,23-25 and 27-29* is/are rejected.

7)☒ Claim(s) *3,4,7,8,10,12,15,20,22 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the amendment, filed 5/3/06.

2. Claims 1-29 are pending.

Response to Arguments

3. Applicant's arguments filed 5/3/06 have been fully considered but they are not persuasive. Applicant argues that Hansen does not suggest teach a first address and control bus connected to the first memory controller. The Examiner disagrees. Hansen teaches a first address and control bus (address bus of buffer 140; Fig. 4) connected to the first memory controller (controller 130). Applicant should note that the claimed language of "connected" is being satisfied by Hansen, who illustrates that the elements are connected/linked/joined to each other (Fig. 1). Since there are no further limitations on the specifics of the connection, Hansen is viewed as teaching this limitation. Applicant also argues that Hansen does not teach a first data bus, which has a shorter data bus symbol time than the symbol time of the address and control bus. Hansen teaches a first data bus (data bus 113), which uses differential clocking on both the rising and falling edges of the input clock (5/20-25). The address and control bus in memory chip 100 of Hansen only samples on the rising edges of the clock (23-25). Thus data bus 113 is faster (shorter symbol time) than address control bus in memory chip 100 since data bus 113 has faster sampling. Therefore, Hansen teaches the claimed first data bus, which has a shorter data bus symbol time than the symbol time of the address and control bus. The previous rejections to the claims are maintained for the above reasons.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,2,5,6,9,11,13,14,16,17,18,19,21,23,24,25,27,28,29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hansen (US 5,778,419).

As to claims 1,5,9:

6. Hansen teaches a memory system comprising: a first memory controller (controller 130; Fig. 1); a first memory component (buffer 150; Fig. 1); a first address and control bus connected to the first memory controller and the first memory component (Fig. 4,6; 7/18-50; 11/40-55); and a first data bus (data bus 113) connected to the first memory controller and to the first memory component (Fig. 1), wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus (5/20-25). The address and control bus in memory chip 100 of Hansen only samples on the rising edges of the clock (23-25). Thus data bus 113 is faster (shorter symbol time) than address control bus in memory chip 100 since data bus 113 has faster sampling.

As to claim 2,6,19:

7. Hansen teaches a second memory component connected to the first address and control bus and to the first data bus (configuration registers; 14/5-17).

As to claim 11,14,16,29:

8. Hansen teaches the first memory controller includes a third termination structure connected to the first data bus (configuration register; 14/5-17).

As to claim 13,17,23,27:

9. Hansen teaches a calibration process is used to adjust a first termination value of the first termination structure (modify bus impedance; 14/5-17).

As to claim 18:

10. Hansen teaches a memory system comprising: a first memory controller (controller 130; Fig. 1); a first memory component (DRAM 140; Fig. 1); a first address and control bus connected to the first memory controller and to the first memory component (Fig. 4,6; 7/18-50; 11/40-55); and a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus(Fig. 1; 5/20-25).

As to claim 21:

11. Hansen teaches a memory system comprising: a first memory controller (controller 130; Fig. 1); a first memory component (DRAM 140; Fig. 1); a first address and control bus connected to the first memory controller and to the first memory component (Fig. 4,6; 7/18-50; 11/40-55); and a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for

first read data sampled from the first data bus and wherein the first data bus uses differential signaling (Fig. 1; 5/20-25).

As to claim 24,28:

12. Hansen teaches the first memory controller contains a first transmit circuit having a first write timing adjustment subcircuit for adjusting a first adjustable write data driving time point for first write data driven on the first data bus (adjust timing; 14/17-33).

As to claim 25:

13. Hansen teaches a memory system comprising: a first memory controller (controller 130; Fig. 1); a first memory component (DRAM 140; Fig. 1); a first address and control bus connected to the first memory controller and to the first memory component (Fig. 4,6; 7/18-50; 11/40-55); and a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus (Fig. 1; 5/20-25) and wherein the first memory component includes a first termination structure connected to the first data bus (configuration register; 14/5-17)..

Allowable Subject Matter

14. Claim 3,4,7,8,10,12,15,20,22,26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. As to claim 3, the prior art does not further suggest a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and has a second data bus symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

16. As to claim 7, the prior art does not teach further comprising: a second memory component connected to the first address and control bus and to the first clock signal conductor; and a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and has a second data bus symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

17. As to claim 10, the prior art does not suggest further comprising: a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second memory component includes a second termination structure connected to the second data bus and wherein the first data bus symbol time is shorter than the first address and control bus symbol time of the first address and control bus.

18. As to claim 15, the prior art does not further teach comprising: a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second memory

component includes a second termination structure connected to the second data bus and wherein the second data bus uses differential signaling.

19. As to claim 20, the prior art does not suggest further comprising: a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and wherein the second memory component accesses a second word stored in the second memory component, the second word being wider than a second data bus width of the second data bus.

20. As to claim 22, the prior art does not suggest further comprising: a second memory component connected to the first address and control bus; and a second data bus connected the first memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second data bus uses differential signaling.

21. As to claim 4,8,12 the prior art does not further teach wherein a quotient of the first data bus symbol time divided by the first address and control bus symbol time is less than or equal to 1/8.

22. As to claim 26, the prior art does not teach further comprising: a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for

adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second memory component includes a second termination structure connected to the second data bus

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Than Nguyen can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen
Primary Examiner
Art Unit 2187